IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 6 and 7 and CANCEL claim 12, without prejudice or disclaimer, in accordance with the following:

1. (**CURRENTLY AMENDED**) A thin film transistor (TFT) comprising:

a channel region having a plurality of primary crystal grain boundaries;

source and drain regions formed at respective ends of the channel region; and

offset regions one of which is formed between the channel region and the source region and the other one of which is formed between the ~~drain regions and the~~ channel region and the drain region,

wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are not positioned in the offset regions, and

wherein a width of each one of the offset regions is smaller than a distance between the primary crystal grain boundaries formed in the channel region.

2. (**CANCELED**)

3. (**ORIGINAL**) The thin film transistor according to claim 1, wherein the polysilicon substrate is formed by a sequential lateral solidification (SLS) method.

4. (**ORIGINAL**) The thin film transistor according to claim 1, wherein the thin film transistor is used in an LCD (liquid crystal display) or organic EL (electroluminescent) device.

5. (**PREVIOUSLY PRESENTED**) The thin film transistor according to claim 1, wherein the primary crystal grain boundaries are substantially perpendicular to a current direction between the source and drain regions of the thin film transistor.

6. (**CURRENTLY AMENDED**) A thin film transistor (TFT) comprising:

a channel region;

source and drain regions respectively formed at opposite sides of the channel region;

~~a~~ lightly doped drain (LDD) ~~region~~ or offset ~~region~~regions ~~respectively~~ formed at respective opposite sides of the channel region and between the source and drain regions ;and

a plurality of primary crystal grain boundaries, wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are positioned in the channel, source and drain regions but not positioned in the LDD or offset ~~region~~regions, and wherein a width of the LDD ~~region~~ or offset ~~region~~regions is less than a distance between two adjoining primary crystal grain boundaries.

7. (**CURRENTLY AMENDED**) A flat panel display device comprising:

a thin film transistor comprising:

a channel region;

offset regions formed at opposite sides of the channel region~~, the offset regions having no doping~~;

source and drain regions respectively formed at outer sides of the offset regions; and

a plurality of primary crystal grain boundaries,

wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are not positioned in the offset regions, and wherein a width of the offset regions, is smaller than a distance between the primary crystal grain boundaries.

8. (**CANCELED**)

9. (**ORIGINAL**) The flat panel display device according to claim 7, wherein the polysilicon substrate is formed by a sequential lateral solidification (SLS) method.

10. (**ORIGINAL**) The flat panel display device according to claim 7, wherein the thin film transistor is used in an LCD (liquid crystal display) or organic EL (electroluminescent) device.

11. (**PREVIOUSLY PRESENTED**) The flat panel display device according to claim 7, wherein the primary crystal grain boundaries are substantially perpendicular to a current direction between the source and drain regions of the thin film transistor.

12 - 14. (**CANCELED**)